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SYSTEM VERIFICATION

PROVING THE DESIGN SOLUTION SATISFIES THE REQUIREMENTS

Academic Press **System Verification: Proving the Design Solution Satisfies the Requirements, Second Edition explains how to determine what verification work must be done, how the total task can be broken down into verification tasks involving six straightforward methods, how to prepare a plan, procedure, and report for each of these tasks, and how to conduct an audit of the content of those reports for a particular product entity. This process-centered book is applicable to engineering and computing projects of all kinds, and the lifecycle approach helps all stakeholders in the design process understand how the verification and validation stage is significant to them. In addition to many flowcharts that illustrate the verification procedures involved, the book also includes 14 verification form templates for use in practice. The author draws on his experience of consulting for industry as well as lecturing to provide a uniquely practical and easy to use guide which is essential reading for systems and validation engineers, as well as everyone involved in the product design process. Includes 14 real life templates for use in verification tasks Explains concepts in the context of the entire design lifecycle, helping all project stakeholders engage Contains a process-focused approach to design model verification that can be applied to all engineering design and software development projects**

VERIFICATION, VALIDATION, AND TESTING OF ENGINEERED SYSTEMS

John Wiley & Sons **Systems' Verification Validation and Testing (VVT) are carried out throughout systems' lifetimes. Notably, quality-cost expended on performing VVT activities and correcting system defects consumes about half of the overall engineering cost. Verification, Validation and Testing of Engineered Systems provides a comprehensive compendium of VVT activities and corresponding VVT methods for implementation throughout the entire lifecycle of an engineered system. In addition, the book strives to alleviate the fundamental testing conundrum, namely: What should be tested? How should one test? When should one test? And, when should one stop testing? In other words, how should one select a VVT strategy and how it be optimized? The book is organized in three parts: The first part provides introductory material about systems and VVT concepts. This part presents a comprehensive explanation of the role of VVT in the process of engineered systems (Chapter-1). The second part describes 40 systems' development VVT activities (Chapter-2) and 27 systems' post-development activities (Chapter-3). Corresponding to these activities, this part also describes 17 non-testing systems' VVT methods (Chapter-4) and 33 testing systems' methods (Chapter-5). The third part of the book describes ways to model systems' quality cost, time and risk (Chapter-6), as well as ways to acquire quality data and optimize the VVT strategy in the face of funding, time and other resource limitations as well as different business objectives (Chapter-7). Finally, this part describes the methodology used to validate the quality model along with a case study describing a system's quality improvements (Chapter-8). Fundamentally, this book is written with two categories of audience in mind. The first category is composed of VVT practitioners, including Systems, Test, Production and Maintenance engineers as well as first and second line managers. The second category is composed of students and faculties of Systems, Electrical, Aerospace, Mechanical and Industrial Engineering schools. This book may be fully covered in two to three graduate level semesters; although parts of the book may be covered in one semester. University instructors will most likely use the book to provide engineering students with knowledge about VVT, as well as to give students an introduction to formal modeling and optimization of VVT strategy.**

FORMAL SYSTEM VERIFICATION

STATE-OF THE-ART AND FUTURE TRENDS

Springer **This book provides readers with a comprehensive introduction to the formal verification of hardware and software. World-leading experts from the domain of formal proof techniques show the latest developments starting from electronic system level (ESL) descriptions down to the register transfer level (RTL). The authors demonstrate at different abstraction layers how formal methods can help to ensure functional correctness. Coverage includes the latest academic research results, as well as descriptions of industrial tools and case studies.**

SYSTEM VALIDATION AND VERIFICATION

CRC Press **Historically, the terms validation and verification have been very loosely defined in the system engineering world, with predictable confusion. Few hardware or software testing texts even touch upon validation and verification, despite the fact that, properly employed, these test tools offer system and test engineers powerful techniques for identifying and solving problems early in the design process. Together, validation and verification encompass testing, analysis, demonstration, and examination methods used to determine whether a proposed design will satisfy system requirements. System Validation and Verification clear definitions of the terms and detailed information on using these fundamental tools for problem solving. It smoothes the transition between requirements and design by providing methods for evaluating the ability of a given approach to satisfy demanding technical requirements. With this book, system and test engineers and project managers gain confidence in their designs and lessen the likelihood of serious problems cropping up late in the program. In addition to explanations of the theories behind the concepts, the book includes practical methods for each step of the process, examples from the author's considerable experience, and illustrations and tables to support the ideas. Although not primarily a textbook, System Validation and Verification is based in part on validation and verification courses taught by the author and is an excellent supplemental reference for engineering students. In addition to its usefulness to system engineers, the book will be valuable to a wider audience including manufacturing, design, software , and risk management project engineers - anyone involved in large systems design projects.**

FORMAL VERIFICATION OF CONTROL SYSTEM SOFTWARE

Princeton University Press **An essential introduction to the analysis and verification of control system software The verification of control system software is critical to a host of technologies and industries, from aeronautics and medical technology to the cars we drive. The failure of controller software can cost people their lives. In this authoritative and accessible book, Pierre-Loïc Garoche provides control engineers and computer scientists with an indispensable introduction to the formal techniques for analyzing and verifying this important class of software. Too often, control engineers are unaware of the issues surrounding the verification of software, while computer scientists tend to be unfamiliar with the specificities of controller software. Garoche provides a unified approach that is geared to graduate students in both fields, covering formal verification methods as well as the design and verification of controllers. He presents a wealth of new verification techniques for performing exhaustive analysis of controller software. These include new means to compute nonlinear invariants, the use of convex optimization tools, and methods for dealing with numerical imprecisions such as floating point computations occurring in the analyzed software. As the autonomy of critical systems continues to increase—as evidenced by autonomous cars, drones, and satellites and landers—the numerical functions in these systems are growing ever more advanced. The techniques presented here are essential to support the formal analysis of the controller software being used in these new and emerging technologies.**

VERIFICATION AND CONTROL OF HYBRID SYSTEMS

A SYMBOLIC APPROACH

Springer Science & Business Media **Hybrid systems describe the interaction of software, described by finite models such as finite-state machines, with the physical world, described by infinite models such as differential equations. This book addresses problems of verification and controller synthesis for hybrid systems. Although these problems are very difficult to solve for general hybrid systems, several authors have identified classes of hybrid systems that admit symbolic or finite models. The novelty of the book lies on the systematic presentation of these classes of hybrid systems along with the relationships between the hybrid systems and the corresponding symbolic models. To show how the existence of symbolic models can be used for verification and controller synthesis, the book also outlines several key results for the verification and controller design of finite systems. Several examples illustrate the different methods and techniques discussed in the book.**

SYSTEMS AND SOFTWARE VERIFICATION

MODEL-CHECKING TECHNIQUES AND TOOLS

Springer Science & Business Media **Model checking is a powerful approach for the formal verification of software. It automatically provides complete proofs of correctness, or explains, via counter-examples, why a system is not correct. Here, the author provides a well written and basic introduction to the new technique. The first part describes in simple terms the theoretical basis of model checking: transition systems as a formal model of systems, temporal logic as a formal language for behavioral properties, and model-checking algorithms. The second part explains how to write rich and structured temporal logic specifications in practice, while the third part surveys some of the major model checkers available.**

VERIFICATION AND VALIDATION IN SYSTEMS ENGINEERING

ASSESSING UML/SYSML DESIGN MODELS

Springer Science & Business Media **At the dawn of the 21st century and the information age, communication and c- puting power are becoming ever increasingly available, virtually pervading almost every aspect of modern socio-economical interactions. Consequently, the potential for realizing a signi?cantly greater number of technology-mediated activities has emerged. Indeed, many of our modern activity ?elds are heavily dependant upon various underlying systems and software-intensive platforms. Such technologies are commonly used in everyday activities such as commuting, traf?c control and m- agement, mobile computing, navigation, mobile communication. Thus, the correct function of the forenamed computing systems becomes a major concern. This is all the more important since, in spite of the numerous updates, patches and ?rmware revisions being constantly issued, newly discovered logical bugs in a wide range of modern software platforms (e. g. , operating systems) and software-intensive systems (e. g. , embedded systems) are just as frequently being reported. In addition, many of today's products and services are presently being deployed in a highly competitive environment wherein a product or service is succeeding in most of the cases thanks to its quality to price ratio for a given set of features. Accordingly, a number of critical aspects have to be considered, such as the ab- ity to pack as many features as needed in a given product or service while c- currently maintaining high quality, reasonable price, and short time -to- market.**

RECONFIGURABLE SYSTEM DESIGN AND VERIFICATION

CRC Press **Reconfigurable systems have pervaded nearly all fields of computation and will continue to do so for the foreseeable future. Reconfigurable System Design and Verification provides a compendium of design and verification techniques for reconfigurable systems, allowing you to quickly search for a technique and determine if it is appropriate to the task at hand. It bridges the gap between the need for reconfigurable computing education and the burgeoning development of numerous different techniques in the design and verification of reconfigurable systems in various application domains. The text explains topics in such a way that they can be immediately grasped and put into practice. It starts with an overview of reconfigurable computing architectures and platforms and demonstrates how to develop reconfigurable systems. This sets up the discussion of the hardware, software, and system techniques that form the core of the text. The authors classify design and verification techniques into primary and secondary categories, allowing the appropriate ones to be easily located and compared. The techniques discussed range from system modeling and system-level design to co-simulation and formal verification. Case studies illustrating real-world applications, detailed explanations of complex algorithms, and self-explaining illustrations add depth to the presentation. Comprehensively covering all techniques related to the hardware-software design and verification of reconfigurable systems, this book provides a single source for information that otherwise would have been dispersed among the literature, making it very difficult to search, compare, and select the technique most suitable. The authors do it all for you, making it easy to find the techniques that fit your system requirements, without having to surf the net or digital libraries to find the candidate techniques and compare them yourself.**

VERIFICATION, VALIDATION AND TESTING OF ENGINEERED SYSTEMS

John Wiley & Sons **Systems' Verification Validation and Testing (VVT) are carried out throughout systems' lifetimes. Notably, quality-cost expended on performing VVT activities and correcting system defects consumes about half of the overall engineering cost. Verification, Validation and Testing of Engineered Systems provides a comprehensive compendium of VVT activities and corresponding VVT methods for implementation throughout the entire lifecycle of an engineered system. In addition, the book strives to alleviate the fundamental testing conundrum, namely: What should be tested? How should one test? When should one test? And, when should one stop testing? In other words, how should one select a VVT strategy and how it be optimized? The book is organized in three parts: The first part provides introductory material about systems and VVT concepts. This part presents a comprehensive explanation of the role of VVT in the process of engineered systems (Chapter-1). The second part describes 40 systems' development VVT activities (Chapter-2) and 27 systems' post-development activities (Chapter-3). Corresponding to these activities, this part also describes 17 non-testing systems' VVT methods (Chapter-4) and 33 testing systems' methods (Chapter-5). The third part of the book describes ways to model systems' quality cost, time and risk (Chapter-6), as well as ways to acquire quality data and optimize the VVT strategy in the face of funding, time and other resource limitations as well as different business objectives (Chapter-7). Finally, this part describes the methodology used to validate the quality model along with a case study describing a system's quality improvements (Chapter-8). Fundamentally, this book is written with two categories of audience in mind. The first category is composed of VVT practitioners, including Systems, Test, Production and Maintenance engineers as well as first and second line managers. The second category is composed of students and faculties of Systems, Electrical, Aerospace, Mechanical and Industrial Engineering schools. This book may be fully covered in two to three graduate level semesters; although parts of the book may be covered in one semester. University instructors will most likely use the book to provide engineering students with knowledge about VVT, as well as to give students an introduction to formal modeling and optimization of VVT strategy.**

SYSTEMVERILOG FOR VERIFICATION

A GUIDE TO LEARNING THE TESTBENCH LANGUAGE FEATURES

Springer Science & Business Media **Based on the highly successful second edition, this extended edition of SystemVerilog for Verification: A Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill. In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students' understanding of the material. Other features of this revision include: New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard Descriptions of UVM features such as factories, the test registry, and the configuration database Expanded code samples and explanations Numerous samples that have been tested on the major SystemVerilog simulators SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.**

VERIFYING CYBER-PHYSICAL SYSTEMS

A PATH TO SAFE AUTONOMY

MIT Press **A graduate-level textbook that presents a unified mathematical framework for modeling and analyzing cyber-physical systems, with a strong focus on verification. Verification aims to establish whether a system meets a set of requirements. For such cyber-physical systems as driverless cars, autonomous spacecraft, and air-traffic management systems, verification is key to building safe systems with high levels of assurance. This graduate-level textbook presents a unified mathematical framework for modeling and analyzing cyber-physical systems, with a strong focus on verification. It distills the ideas and algorithms that have emerged from more than three decades of research and have led to the creation of industrial-scale modeling and verification techniques for cyber-physical systems.**

HIGH-LEVEL VERIFICATION

METHODS AND TOOLS FOR VERIFICATION OF SYSTEM-LEVEL DESIGNS

Springer Science & Business Media **Given the growing size and heterogeneity of Systems on Chip (SOC), the design process from initial specification to chip fabrication has become increasingly complex. This growing complexity provides incentive for designers to use high-level languages such as C, SystemC, and SystemVerilog for system-level design. While a major goal of these high-level languages is to enable verification at a higher level of abstraction, allowing early exploration of system-level designs, the focus so far for validation purposes has been on traditional testing techniques such as random testing and scenario-based testing. This book focuses on high-level verification, presenting a design methodology that relies upon advances in synthesis techniques as well as on incremental refinement of the design process. These refinements can be done manually or through elaboration tools. This book discusses verification of specific properties in designs written using high-level languages, as well as checking that the refined implementations are equivalent to their high-level specifications. The novelty of each of these techniques is that they use a combination of formal techniques to do scalable verification of system designs completely automatically. The verification techniques presented in this book include methods for verifying properties of high-level designs and methods for verifying that the translation from high-level design to a low-level Register Transfer Language (RTL) design preserves semantics. Used together, these techniques guarantee that properties verified in the high-level design are preserved through the translation to low-level RTL.**

VERIFICATION AND VALIDATION IN SYSTEMS ENGINEERING

ASSESSING UML/SYSML DESIGN MODELS

Springer **At the dawn of the 21st century and the information age, communication and c- puting power are becoming ever increasingly available, virtually pervading almost every aspect of modern socio-economical interactions. Consequently, the potential for realizing a signi?cantly greater number of technology-mediated activities has emerged. Indeed, many of our modern activity ?elds are heavily dependant upon various underlying systems and software-intensive platforms. Such technologies are commonly used in everyday activities such as commuting, traf?c control and m- agement, mobile computing, navigation, mobile communication. Thus, the correct function of the forenamed computing systems becomes a major concern. This is all the more important since, in spite of the numerous updates, patches and ?rmware revisions being constantly issued, newly discovered logical bugs in a wide range of modern software platforms (e. g. , operating systems) and software-intensive systems (e. g. , embedded systems) are just as frequently being reported. In addition, many of today's products and services are presently being deployed in a highly competitive environment wherein a product or service is succeeding in most of the cases thanks to its quality to price ratio for a given set of features. Accordingly, a number of critical aspects have to be considered, such as the ab- ity to pack as many features as needed in a given product or service while c- currently maintaining high quality, reasonable price, and short time -to- market.**

SYSTEM-ON-A-CHIP VERIFICATION

METHODOLOGY AND TECHNIQUES

Springer Science & Business Media **This is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign-off. All the verification aspects in this exciting new book are illustrated with a single reference design for Bluetooth application.**

TEMPORAL VERIFICATION OF REACTIVE SYSTEMS

SAFETY

Springer Science & Business Media **This book is about the verification of reactive systems. A reactive system is a system that maintains an ongoing interaction with its environment, as opposed to computing some final value on termination. The family of reactive systems includes many classes of programs whose correct and reliable construction is con sidered to be particularly challenging, including concurrent programs, embedded and process control programs, and operating systems. Typical examples of such systems are an air traffic control system, programs controlling mechanical devices such as a train, or perpetually ongoing processes such as a nuclear reactor. With the expanding use of computers in safety-critical areas, where failure is potentially disastrous, correctness is crucial. This has led to the introduction of formal verification techniques, which give both users and designers of software and hardware systems greater confidence that the systems they build meet the desired specifications. Framework The approach promoted in this book is based on the use of temporal logic for specifying properties of reactive systems, and develops an extensive verification methodology for proving that a system meets its temporal specification. Reactive programs must be specified in terms of their ongoing behavior, and temporal logic provides an expressive and natural language for specifying this behavior. Our framework for specifying and verifying temporal properties of reactive systems is based on the following four components: 1. A computational model to describe the behavior of reactive systems. The model adopted in this book is that of a Fair Transition System (FTS).**

COMPREHENSIVE FUNCTIONAL VERIFICATION

THE COMPLETE INDUSTRY CYCLE

Elsevier **One of the biggest challenges in chip and system design is determining whether the hardware works correctly. That is the job of functional verification engineers and they are the audience for this comprehensive text from three top industry professionals. As designs increase in complexity, so has the value of verification engineers within the hardware design team. In fact, the need for skilled verification engineers has grown dramatically--functional verification now consumes between 40 and 70% of a project's labor, and about half its cost. Currently there are very few books on verification for engineers, and none that cover the subject as comprehensively as this text. A key strength of this book is that it describes the entire verification cycle and details each stage. The organization of the book follows the cycle, demonstrating how functional verification engages all aspects of the overall design effort and how individual cycle stages relate to the larger design process. Throughout the text, the authors leverage their 35 plus years experience in functional verification, providing examples and case studies, and focusing on the skills, methods, and tools needed to complete each verification task. Comprehensive overview of the complete verification cycle Combines industry experience with a strong emphasis on functional verification fundamentals Includes real-world case studies**

BIOMETRIC TECHNOLOGIES AND VERIFICATION SYSTEMS

Elsevier **Biometric Technologies and Verification Systems is organized into nine parts composed of 30 chapters, including an extensive glossary of biometric terms and acronyms. It discusses the current state-of-the-art in biometric verification/authentication, identification and system design principles. It also provides a step-by-step discussion of how biometrics works; how biometric data in human beings can be collected and analyzed in a number of ways; how biometrics are currently being used as a method of personal identification in which people are recognized by their own unique corporal or behavioral characteristics; and how to create detailed menus for designing a biometric verification system. Only biometrics verification/authentication is based on the identification of an intrinsic part of a human being. Tokens, such as smart cards, magnetic stripe cards, and physical keys can be lost, stolen, or duplicated. Passwords can be forgotten, shared, or unintentionally observed by a third party. Forgotten passwords and lost "smart cards" are a nuisance for users and an expensive time-waster for system administrators. Biometric security solutions offer some unique advantages for identifying and verifying/ authenticating human beings over more traditional security methods. This book will serve to identify the various security applications biometrics can play a highly secure and specific role in. * Contains elements such as Sidebars, Tips, Notes and URL links * Heavily illustrated with over 150 illustrations, screen captures, and photographs * Details the various biometric technologies and how they work while providing a discussion of the economics, privacy issues and challenges of implementing biometric security solutions**

VERIFICATION OF REACTIVE SYSTEMS

FORMAL METHODS AND ALGORITHMS

Springer Science & Business Media **This book is a solid foundation of the most important formalisms used for specification and verification of reactive systems. In particular, the text presents all important results on m-calculus, w-automata, and temporal logics, shows the relationships between these formalisms and describes state-of-the-art verification procedures for them. It also discusses advantages and disadvantages of these formalisms, and shows up their strengths and weaknesses. Most results are given with detailed proofs, so that the presentation is almost self-contained. Includes all definitions without relying on other material Proves all theorems in detail Presents detailed algorithms in pseudo-code for verification as well as translations to other formalisms**

SYSTEM-ON-A-CHIP VERIFICATION

METHODOLOGY AND TECHNIQUES

Springer Science & Business Media **This is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign-off. All the verification aspects in this exciting new book are illustrated with a single reference design for Bluetooth application.**

REACTIVE SYSTEMS

MODELLING, SPECIFICATION AND VERIFICATION

Cambridge University Press **Formal methods is the term used to describe the specification and verification of software and software systems using mathematical logic. Various methodologies have been developed and incorporated into software tools. An important subclass is distributed systems. There are many books that look at particular methodologies for such systems, e.g. CSP, process algebra. This book offers a more balanced introduction for graduate students that describes the various approaches, their strengths and weaknesses, and when they are best used. Milner's CCS and its operational semantics are introduced, together with notions of behavioural equivalence based on bisimulation techniques and with variants of Hennessy-Milner modal logics. Later in the book, the presented theories are extended to take timing issues into account. The book has arisen from various courses taught in Iceland and Denmark and is designed to give students a broad introduction to the area, with exercises throughout.**

REAL-TIME SYSTEMS

SCHEDULING, ANALYSIS, AND VERIFICATION

John Wiley & Sons **The first book to provide a comprehensive overview of the subject rather than a collection of papers. The author is a recognized authority in the field as well as an outstanding teacher lauded for his ability to convey these concepts clearly to many different audiences. A handy reference for practitioners in the field.**

VERIFICATION OF DIGITAL AND HYBRID SYSTEMS

Springer Science & Business Media **This book grew out of a NATO Advanced Study Institute summer school that was held in Antalya, TUrkey from 26 May to 6 June 1997. The purpose of the summer school was to expose recent advances in the formal verification of systems composed of both logical and continuous time components. The course was structured in two parts. The first part covered theorem-proving, system automaton models, logics, tools, and complexity of verification. The second part covered modeling and verification of hybrid systems, i. e. , systems composed of a discrete event part and a continuous time part that interact with each other in novel ways. Along with advances in microelectronics, methods to design and build logical systems have grown progressively complex. One way to tackle the problem of ensuring the error-free operation of digital or hybrid systems is through the use of formal techniques. The exercise of comparing the formal specification of a logical system namely, what it is supposed to do to its formal operational description-what it actually does!-in an automated or semi-automated manner is called verification. Verification can be performed in an after-the-fact manner, meaning that after a system is already designed, its specification and operational description are regenerated or modified, if necessary, to match the verification tool at hand and the consistency check is carried out.**

VERIFICATION AND EVALUATION OF COMPUTER AND COMMUNICATION SYSTEMS

11TH INTERNATIONAL CONFERENCE, VECOS 2017, MONTREAL, QC, CANADA, AUGUST 24–25, 2017, PROCEEDINGS

Springer **This book constitutes the proceedings of the 11th International Conference International Conference on Verification and Evaluation of Computer and Communication Systems (VECoS 2017), held at Concordia University, Montreal, Canada, in August 2017. The 13 full papers, together with 3 abstracts in this volume were carefully reviewed and selected from 35 submissions. The aim of the VECoS conference is to bring together researchers and practitioners in the areas of verification, control, performance and dependability evaluation in order to discuss state-of-the-art and challenges in modern computer and communication systems in which functional and extra-functional properties are strongly interrelated. Thus, the main motivation for VECoS is to encourage the cross-fertilization between various formal verification and evaluation approaches, methods and techniques,**

and especially those developed for concurrent and dis-tributed hardware/software systems.

THE FUNCTIONAL VERIFICATION OF ELECTRONIC SYSTEMS

AN OVERVIEW FROM VARIOUS POINTS OF VIEW

Intl. Engineering Consortiu **Addressing the need for full and accurate functional information during the design process, this guide offers a comprehensive overview of functional verification from the points of view of leading experts at work in the electronic-design industry.**

DIGITAL SYSTEM VERIFICATION

A COMBINED FORMAL METHODS AND SIMULATION FRAMEWORK

Springer Nature **Integrated circuit capacity follows Moore's law, and chips are commonly produced at the time of this writing with over 70 million gates per device. Ensuring correct functional behavior of such large designs before fabrication poses an extremely challenging problem. Formal verification validates the correctness of the implementation of a design with respect to its specification through mathematical proof techniques. Formal techniques have been emerging as commercialized EDA tools in the past decade. Simulation remains a predominantly used tool to validate a design in industry. After more than 50 years of development, simulation methods have reached a degree of maturity, however, new advances continue to be developed in the area. A simulation approach for functional verification can theoretically validate all possible behaviors of a design but requires excessive computational resources. Rapidly evolving markets demand short design cycles while the increasing complexity of a design causes simulation approaches to provide less and less coverage. Formal verification is an attractive alternative since 100% coverage can be achieved; however, large designs impose unrealistic computational requirements. Combining formal verification and simulation into a single integrated circuit validation framework is an attractive alternative. This book focuses on an Integrated Design Validation (IDV) system that provides a framework for design validation and takes advantage of current technology in the areas of simulation and formal verification resulting in a practical validation engine with reasonable runtime. After surveying the basic principles of formal verification and simulation, this book describes the IDV approach to integrated circuit functional validation. Table of Contents: Introduction / Formal Methods Background / Simulation Approaches / Integrated Design Validation System / Conclusion and Summary**

MEDICAL DEVICE SOFTWARE VERIFICATION, VALIDATION AND COMPLIANCE

Artech House **HereOCOs the first book written specifically to help medical device and software engineers, QA and compliance professionals, and corporate business managers better understand and implement critical verification and validation processes for medical device software.Offering you a much broader, higher-level picture than other books in this field, this book helps you think critically about software validation -- to build confidence in your softwareOCOs safety and effectiveness. The book presents validation activities for each phase of the development lifecycle and shows: why these activities are important and add value; how to undertake them; and what outputs need to be created to document the validation process.From software embedded within medical devices, to software that performs as a medical device itself, this comprehensive book explains how properly handled validation throughout the development lifecycle can help bring medical devices to completion sooner, at higher quality, in compliance with regulations."**

HARDWARE VERIFICATION WITH SYSTEM VERILOG

AN OBJECT-ORIENTED FRAMEWORK

Springer Science & Business Media **Verification is increasingly complex, and SystemVerilog is one of the languages that the verification community is turning to. However, no language by itself can guarantee success without proper techniques. Object-oriented programming (OOP), with its focus on managing complexity, is ideally suited to this task. With this handbook—the first to focus on applying OOP to SystemVerilog—we'll show how to manage complexity by using layers of abstraction and base classes. By adapting these techniques, you will write more "reasonable" code, and build efficient and reusable verification components. Both a learning tool and a reference, this handbook contains hundreds of real-world code snippets and three professional verification-system examples. You can copy and paste from these examples, which are all based on an open-source, vendor-neutral framework (with code freely available at www.trusster.com). Learn about OOP techniques such as these: Creating classes—code interfaces, factory functions, reuse Connecting classes—pointers, inheritance, channels Using "correct by construction"—strong typing, base classes Packaging it up—singletons, static methods, packages**

EMBEDDED SYSTEM DESIGN

MODELING, SYNTHESIS AND VERIFICATION

Springer Science & Business Media **Embedded System Design: Modeling, Synthesis and Verification introduces a model-based approach to system level design. It presents modeling techniques for both computation and communication at different levels of abstraction, such as specification, transaction level and cycle-accurate level. It discusses synthesis methods for system level architectures, embedded software and hardware components. Using these methods, designers can develop applications with high level models, which are automatically translatable to low level implementations. This book, furthermore, describes simulation-based and formal verification methods that are essential for achieving design confidence. The book concludes with an overview of existing tools along with a design case study outlining the practice of embedded system design. Specifically, this book addresses the following topics in detail: . System modeling at different abstraction levels . Model-based system design . Hardware/Software codesign . Software and Hardware component synthesis . System verification This book is for groups within the embedded system community: students in courses on embedded systems, embedded application developers, system designers and managers, CAD tool developers, design automation, and system engineering.**

LOVE FOR FORENINGEN TIL KVÆGAVLENS FREMME I GAMMEL SOGN

SPECIFICATION AND COMPOSITIONAL VERIFICATION OF REAL-TIME SYSTEMS

Springer Science & Business Media **This monograph presents two formal methods for the specification and compositional verification of real-time systems. One uses a real-time extension of temporal logic and the other is based on extended Hoare triples. Programs consist of concurrent processes with synchronous message passing. The maximal parallelism model is extended to multiprogramming.**

SYSTEM-ON-CHIP SECURITY

VALIDATION AND VERIFICATION

Springer Nature **This book describes a wide variety of System-on-Chip (SoC) security threats and vulnerabilities, as well as their sources, in each stage of a design life cycle. The authors discuss a wide variety of state-of-the-art security verification and validation approaches such as formal methods and side-channel analysis, as well as simulation-based security and trust validation approaches. This book provides a comprehensive reference for system on chip designers and verification and validation engineers interested in verifying security and trust of heterogeneous SoCs.**

SEMI-PHYSICAL VERIFICATION TECHNOLOGY FOR DYNAMIC PERFORMANCE OF INTERNET OF THINGS SYSTEM

Springer **This book combines semi-physical simulation technology with an Internet of Things (IOT) application system based on novel mathematical methods such as the Fisher matrix, artificial neural networks, thermodynamic analysis, support vector machines, and image processing algorithms. The dynamic testing and semi-physical verification of the theory and application were conducted for typical IOT systems such as RFID systems, Internet of Vehicles systems, and two-dimensional barcode recognition systems. The findings presented are of great scientific significance and have wide application potential for solving bottlenecks in the development of RFID technology and IOT engineering. The book is a valuable resource for postgraduate students in fields such as computer science and technology, control science and engineering, and information science. Moreover, it is a useful reference resource for researchers in IOT and RFID-related industries, logistics practitioners, and system integrators.**

TAXONOMIES FOR THE DEVELOPMENT AND VERIFICATION OF DIGITAL SYSTEMS

Springer Science & Business Media **Thorough set of definitions for the terms and models used in the creation, refinement, and verification of complex systems from the conceptual level down to its implementation Considering both the hardware and software components of the system Also covers the emerging area of platform-based design Provides both knowledge of models and terms, and understanding of these models and how they are used.**

FORMAL MODELING AND VERIFICATION OF CYBER-PHYSICAL SYSTEMS

1ST INTERNATIONAL SUMMER SCHOOL ON METHODS AND TOOLS FOR THE DESIGN OF DIGITAL SYSTEMS, BREMEN, GERMANY, SEPTEMBER 2015

Springer **This book presents the lecture notes of the 1st Summer School on Methods and Tools for the Design of Digital Systems, 2015, held in Bremen, Germany. The topic of the summer school was devoted to modeling and verification of cyber-physical systems. This covers several aspects of the field, including hybrid systems and model checking, as well as applications in robotics and aerospace systems. The main chapters have been written by leading scientists, who present their field of research, each providing references to introductory material as well as latest scientific advances and future research directions. This is complemented by short papers submitted by the participating PhD students.**

VERIFICATION TECHNIQUES FOR SYSTEM-LEVEL DESIGN

Morgan Kaufmann **This book will explain how to verify SoC (Systems on Chip) logic designs using “formal and “semiformal verification techniques. The critical issue to be addressed is whether the functionality of the design is the one that the designers intended. Simulation has been used for checking the correctness of SoC designs (as in “functional verification), but many subtle design errors cannot be caught by simulation. Recently, formal verification, giving mathematical proof of the correctness of designs, has been gaining popularity. For higher design productivity, it is essential to debug designs as early as possible, which this book facilitates. This book covers all aspects of high-level formal and semiformal verification techniques for system level designs. • First book that covers all aspects of formal and semiformal, high-level (higher than RTL) design verification targeting SoC designs. • Formal verification of high-level designs (RTL or higher). • Verification techniques are discussed with associated system-level design methodology.**

VERIFICATION AND EVALUATION OF COMPUTER AND COMMUNICATION SYSTEMS

13TH INTERNATIONAL CONFERENCE, VECOS 2019, PORTO, PORTUGAL, OCTOBER 9, 2019, PROCEEDINGS

Springer Nature **This book constitutes the proceedings of the 13th International Conference on Verification and Evaluation of Computer and Communication Systems (VECoS 2019), held in Porto, Portugal, in October 2019. The 7 full papers in this volume, presented together with two invited talks, were carefully reviewed and selected from 13 submissions. The aim of the VECoS conference is to bring together researchers and practitioners in the areas of verification, control, performance, and dependability evaluation in order to discuss state of the art and challenges in modern computer and communication systems in which functional and extra-functional properties are strongly interrelated. Thus, the main motivation for VECoS is to encourage the cross-fertilization between various formal verification and evaluation approaches, methods and techniques, and especially those developed for concurrent and distributed hardware/software systems.**

COMPUTER AIDED VERIFICATION

3RD INTERNATIONAL WORKSHOP, CAV '91, AALBORG, DENMARK, JULY 1-4, 1991. PROCEEDINGS

Springer Science & Business Media **This volume contains the proceedings of a workshop on computer aided verification. Topics include verification and validation tools for hardware and software, verification methods, and verification theories and their applicability.**

ELECTRONIC DESIGN AUTOMATION FOR IC SYSTEM DESIGN, VERIFICATION, AND TESTING

CRC Press **The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC System Design, Verification, and Testing thoroughly examines system-level design, microarchitectural design, logic verification, and testing. Chapters contributed by leading experts authoritatively discuss processor modeling and design tools, using performance metrics to select microprocessor cores for integrated circuit (IC) designs, design and verification languages, digital simulation, hardware acceleration and emulation, and much more. New to This Edition: Major updates appearing in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition—these are illustrated by new chapters on high-level synthesis, system-on-chip (SoC) block-based design, and back-annotating system-level models Offering improved depth and modernity, Electronic Design Automation for IC System Design, Verification, and Testing provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals.**

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