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KEY=COMPREHENSIVE - ADRIEL PHELPS

Comprehensive Functional Verification

The Complete Industry Cycle

Morgan Kaufmann One of the biggest challenges in chip and system design is determining whether the hardware works correctly. That is the job of functional verification engineers and they are the audience for this comprehensive text from three top industry professionals. As designs increase in complexity, so has the value of verification engineers within the hardware design team. In fact, the need for skilled verification engineers has grown dramatically--functional verification now consumes between 40 and 70% of a project's labor, and about half its cost. Currently there are very few books on verification for engineers, and none that cover the subject as comprehensively as this text. A key strength of this book is that it describes the entire verification cycle and details each stage. The organization of the book follows the cycle, demonstrating how functional verification engages all aspects of the overall design effort and how individual cycle stages relate to the larger design process. Throughout the text, the authors leverage their 35 plus years experience in functional verification, providing examples and case studies, and focusing on the skills, methods, and tools needed to complete each verification task. Comprehensive overview of the complete verification cycle Combines industry experience with a strong emphasis on functional verification fundamentals Includes real-world case studies

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Elsevier One of the biggest challenges in chip and system design is determining whether the hardware works correctly. That is the job of functional verification engineers and they are the audience for this comprehensive text from three top industry professionals. As designs increase in complexity, so has the value of verification engineers within the hardware design team. In fact, the need for skilled verification engineers has grown dramatically--functional verification now consumes between 40 and 70% of a project's labor, and about half its cost. Currently there are very few books on verification for engineers, and none that cover the subject as comprehensively as this text. A key strength of this book is that it describes the entire verification cycle and details each stage. The organization of the book follows the cycle, demonstrating how functional verification engages all aspects of the overall design effort and how individual cycle stages relate to the larger design process. Throughout the text, the authors leverage their 35 plus years experience in functional verification, providing examples and case studies, and focusing on the skills, methods, and tools needed to complete each verification task. Comprehensive overview of the complete verification cycle Combines industry experience with a strong emphasis on functional verification fundamentals Includes real-world case studies

Functional Verification Coverage Measurement and Analysis

Springer Science & Business Media This book addresses a means of quantitatively assessing functional verification progress. Without this process, design and verification engineers, and their management, are left guessing whether or not they have completed verifying the device they are designing. Using the techniques described in this book, they will learn how to build a toolset which allows them to know how close they are to functional closure. This is the first book to introduce a useful taxonomy for coverage of metric classification. Using this taxonomy, the reader will clearly understand the process of creating an effective coverage model. This book offers a thoughtful and comprehensive treatment of its subject for anybody who is really serious about functional verification.

ASIC/SoC Functional Design Verification

A Comprehensive Guide to Technologies and Methodologies

Springer This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon. The author first outlines all of the verification sub-fields at a high level, with just enough depth to allow an engineer to grasp the field before delving into its detail. He then describes in detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven Verification), Low Power Verification (Unified Power Format UPF), AMS (Analog Mixed Signal) verification, Virtual Platform TLM2.0/ESL (Electronic System Level) methodology, Static Formal Verification, Logic Equivalency Check (LEC), Hardware Acceleration, Hardware Emulation, Hardware/Software Co-verification, Power Performance Area (PPA) analysis on a virtual platform, Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies.

The Functional Verification of Electronic Systems

An Overview from Various Points of View

Intl. Engineering Consortiu Addressing the need for full and accurate functional information during the design process, this guide offers a comprehensive overview of functional verification from the points of view of leading experts at work in the electronic-design industry.

Standardized Functional Verification

Springer Science & Business Media The Integrated Circuit (IC) industry has gone without a standardized verification approach for decades. This book defines a uniform, standardizable methodology for verifying the logical behavior of an integrated circuit, whether an I/O controller, a microprocessor, or a complete digital system. This book will help Engineers and managers responsible for IC development to bring a single, standards-based methodology to their R & D efforts, cutting costs and improving results.

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System-on-a-Chip Verification

Methodology and Techniques

Springer Science & Business Media This is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign-off. All the verification aspects in this exciting new book are illustrated with a single reference design for Bluetooth application.

Functional Verification of Programmable Embedded Architectures

A Top-Down Approach

Springer Science & Business Media Validation of programmable architectures, consisting of processor cores, coprocessors, and memory subsystems, is one of the major bottlenecks in current System-on-Chip design methodology. A critical challenge in validation of such systems is the lack of a golden reference model. As a result, many existing validation techniques employ a bottom-up approach to design verification, where the functionality of an existing architecture is, in essence, reverse-engineered from its implementation. Traditional validation techniques employ different reference models depending on the abstraction level and verification task, resulting in potential inconsistencies between multiple reference models. This book presents a top-down validation methodology that complements the existing bottom-up approaches. It leverages the system architect's knowledge about the behavior of the design through architecture specification using an Architecture Description Language (ADL). The authors also address two fundamental challenges in functional verification: lack of a golden reference model, and lack of a comprehensive functional coverage metric. Functional Verification of Programmable Embedded Architectures: A Top-Down Approach is designed for students, researchers, CAD tool developers, designers, and managers interested in the development of tools, techniques and methodologies for system-level design, microprocessor validation, design space exploration and functional verification of embedded systems.

Advanced Verification Techniques

A SystemC Based Approach for Successful Tapeout

Springer Science & Business Media "As chip size and complexity continues to grow exponentially, the challenges of functional verification are becoming a critical issue in the electronics industry. It is now commonly heard that logical errors missed during functional verification are the most common cause of chip re-spins, and that the costs associated with functional verification are now outweighing the costs of chip design. To cope with these challenges engineers are increasingly relying on new design and verification methodologies and languages. Transaction-based design and verification, constrained random stimulus generation, functional coverage analysis, and assertion-based verification are all techniques that advanced design and verification teams routinely use today. Engineers are also increasingly turning to design and verification models based on C/C++ and SystemC in order to build more abstract, higher performance hardware and software models and to escape the limitations of RTL HDLs. This new book, Advanced Verification Techniques, provides specific guidance for these advanced verification techniques. The book includes realistic examples and shows how SystemC and SCV can be applied to a variety of advanced design and verification tasks." - Stuart Swan

Metric Driven Design Verification

An Engineer's and Executive's Guide to First Pass Success

Springer Science & Business Media The purpose of the book is to train verification engineers on the breadth of technologies available and to give them a utilitarian methodology for making effective use of those technologies. The book is easy to understand and a joy to read. Its organization follows a 'typical' verification project from inception to completion, (planning to closure). The book elucidates concepts using non-technical terms and clear entertaining explanations. Analogies to other fields are employed to keep the book light-hearted and interesting.

Complete Functional Verification of Problem-oriented Protocols

Professional Verification

A Guide to Advanced Functional Verification

Springer Science & Business Media Professional Verification is a guide to advanced functional verification in the nanometer era. It presents the best practices in functional verification used today and provides insights on how to solve the problems that verification teams face. Professional Verification is based on the experiences of advanced verification teams throughout the industry, along with work done at Cadence Design Systems. Professional Verification presents a complete and detailed Unified Verification Methodology based on the best practices in use today. It also addresses topics important to those doing advanced functional verification, such as assertions, functional coverage, formal verification, and reactive testbenches.

Complete Functional Verification

Formal System Verification

State-of the-Art and Future Trends

Springer This book provides readers with a comprehensive introduction to the formal verification of hardware and software. World-leading experts from the domain of formal proof techniques show the latest developments starting from electronic system level (ESL) descriptions down to the register transfer level (RTL). The authors demonstrate at different abstraction layers how formal methods can help to ensure functional correctness. Coverage includes the latest academic research results, as well as descriptions of industrial tools and case studies.

Verification Methodology Manual for SystemVerilog

Springer Science & Business Media Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly. Unique in its broad coverage of SystemVerilog, advanced functional verification, and the combination of the two.

Hardware Design Verification

Simulation and Formal Method-based Approaches

Prentice Hall The Practical, Start-to-Finish Guide to Modern Digital Design Verification As digital logic designs grow larger and more complex, functional verification has become the number one bottleneck in the design process. Reducing verification time is crucial to project success, yet many practicing engineers have had little formal training in verification, and little exposure to the newest solutions.Hardware Design Verificationsystematically presents today's most valuable simulation-based and formal verification techniques, helping test and design engineers choose the best approach for each project, quickly gain confidence in their designs, and move into fabrication far more rapidly. College students will find that coverage of verification principles and common industry practices will help them prepare for jobs as future verification engineers. Author William K. Lam, one of the world's leading experts in design verification, is a recent winner of the Chairman's Award for Innovation, Sun Microsystems' most prestigious technical achievement award. Drawing on his wide-ranging experience, he introduces the foundational principles of verification, presents traditional techniques that have survived the test of time, and introduces emerging techniques for today's most challenging designs. Throughout, Lam emphasizes practical examples rather than mathematical proofs; wherever advanced math is essential, he explains it clearly and accessibly. Coverage includes Simulation-based versus formal verification: advantages, disadvantages, and tradeoffs Coding for verification: functional and timing correctness, syntactical and structure checks, simulation performance, and more Simulator architectures and operations, including event-driven, cycle-based, hybrid, and hardware-based simulators Testbench organization, design, and tools: creating a fast, efficient test environment Test scenarios and assertion: planning, test cases, test generators, commercial and Verilog assertions, and more Ensuring complete coverage, including code, parameters, functions, items, and cross-coverage The verification cycle: failure capture, scope reduction, bug tracking, simulation data dumping, isolation of underlying causes, revision control, regression, release mechanisms, and tape-out criteria An accessible introduction to the mathematics and algorithms of formal verification, from Boolean functions to state-machine equivalence and graph algorithms Decision diagrams, equivalence checking, and symbolic simulation Model checking and symbolic computation Simply put,Hardware Design Verificationwill help you improve and accelerate your entire verification process--from planning through tape-out--so you can get to market faster with higher quality designs.

Finding Your Way Through Formal Verification

Createspace Independent Publishing Platform There are already many books on formal verification, from academic to application-centric, and from tutorials for beginners to guides for advanced users. Many are excellent for their intended purpose; we recommend a few at the end of this book. But most start from the assumption that you have already committed to becoming a hands-on expert (or in some cases that you already are an expert). We feel that detailed tutorials are not the easiest place to extract the introductory view many of us are looking for - background, a general idea of how methods work, applications and how formal verification is managed in the overall verification objective. Since we're writing for a fairly wide audience, we cover some topics that some of you may consider elementary (why verification is hard), some we hope will be of general interest (elementary understanding of the technology) and others that may not immediately interest some readers (setting up a formal verification team). What we intentionally do not cover at all is how to become a hands-on expert.

Writing Testbenches: Functional Verification of HDL Models

Springer Science & Business Media mental improvements during the same period. What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough. In the second edition of Writing Testbenches, Bergeron raises the verification level of abstraction by introducing coverage-driven constrained-random transaction-level self-checking testbenches all made possible through the introduction of hardware verification languages (HVLs), such as e from Verisity and OpenVera from Synopsys. The state-of-art methodologies described in Writing Test benches will contribute greatly to the much-needed equivalent of a synthesis breakthrough in verification productivity. I not only highly recommend this book, but also I think it should be required reading by anyone involved in design and verification of today's ASIC, SoCs and systems. Harry Foster Chief Architect Verplex Systems, Inc. xviii Writing Testbenches: Functional Verification of HDL Models PREFACE If you survey hardware design groups, you will learn that between 60% and 80% of their effort is now dedicated to verification.

Assertion-Based Design

Springer Science & Business Media There is much excitement in the design and verification community about assertion-based design. The question is, who should study assertion-based design? The emphatic answer is, both design and verification engineers. What may be unintuitive to many design engineers is that adding assertions to RTL code will actually reduce design time, while better documenting design intent. Every design engineer should read this book! Design engineers that add assertions to their design will not only reduce the time needed to complete a design, they will also reduce the number of interruptions from verification engineers to answer questions about design intent and to address verification suite mistakes. With design assertions in place, the majority of the interruptions from verification engineers will be related to actual design problems and the error feedback provided will be more useful to help identify design flaws. A design engineer who does not add assertions to the RTL code will spend more time with verification engineers explaining the design functionality and intended interface requirements, knowledge that is needed by the verification engineer to complete the job of testing the design.

Effective Functional Verification

Principles and Processes

Springer Science & Business Media Effective Functional Verification is organized into 4 parts. The first part contains 3 chapters designed appeal to newcomers and experienced people to the field. There is a survey of various verification methodologies and a discussion of them. The second part with 3 chapters is targeted towards people in management and higher up on the experience ladders. New verification engineers reading these chapters learn what is expected and how things work in verification. Some case studies are also presented with analysis of proposed improvements. The last two parts are the result of experience of several years. It goes into how to optimize a verification plan and an environment and how to get results effectively. Various subjects are discussed here to get the most out of a verification environment. Lastly, the appendix discusses some tool specifics to help remove repetitive work and also some tool specific guidelines. While reading Effective Functional Verification, one will be able to get a jump start on planning and executing a verification plan using the concepts presented.

Functional Verification A Complete Guide - 2020 Edition

5starcooks How do you maintain Functional verification's Integrity? Are you dealing with any of the same issues today as yesterday? What can you do about this? What do your reports reflect? Have you identified breakpoints and/or risk tolerances that will trigger broad consideration of a potential need for intervention or modification of strategy? Is your basic point _____ or _____? This exclusive Functional Verification self-assessment will make you the accepted Functional Verification domain visionary by revealing just what you need to know to be fluent and ready for any Functional Verification challenge. How do I reduce the effort in the Functional Verification work to be done to get problems solved? How can I ensure that plans of action include every Functional Verification task and that every Functional Verification outcome is in place? How will I save time investigating strategic and tactical options and ensuring Functional Verification costs are low? How can I deliver tailored Functional Verification advice instantly with structured going-forward plans? There's no better guide through these mind-expanding questions than acclaimed best-selling author Gerard Blokdyk. Blokdyk ensures all Functional Verification essentials are covered, from every angle: the Functional Verification self-assessment shows succinctly and clearly that what needs to be clarified to organize the required activities and processes so that Functional Verification outcomes are achieved. Contains extensive criteria grounded in past and current successful projects and activities by experienced Functional Verification practitioners. Their mastery, combined with the easy elegance of the self-assessment, provides its superior value to you in knowing how to ensure the outcome of any efforts in Functional Verification are maximized with professional results. Your purchase includes access details to the Functional Verification self-assessment dashboard download which gives you your dynamically prioritized projects-ready tool and shows you exactly what to do next. Your exclusive instant access details can be found in your book. You will receive the following contents with New and Updated specific criteria: - The latest quick edition of the book in PDF - The latest complete edition of the book in PDF, which criteria correspond to the criteria in... - The Self-Assessment Excel Dashboard - Example pre-filled Self-Assessment Excel Dashboard to get familiar with results generation - In-depth and specific Functional Verification Checklists - Project management checklists and templates to assist with implementation INCLUDES LIFETIME SELF ASSESSMENT UPDATES Every self assessment comes with Lifetime Updates and Lifetime Free Updated Books. Lifetime Updates is an industry-first feature which allows you to receive verified self assessment updates, ensuring you always have the most accurate information at your fingertips.

Verification, Validation, and Testing of Engineered Systems

John Wiley & Sons Systems' Verification Validation and Testing (VVT) are carried out throughout systems' lifetimes. Notably, quality-cost expended on performing VVT activities and correcting system defects consumes about half of the overall engineering cost. Verification, Validation and Testing of Engineered Systems provides a comprehensive compendium of VVT activities and corresponding VVT methods for implementation throughout the entire lifecycle of an engineered system. In addition, the book strives to alleviate the fundamental testing conundrum, namely: What should be tested? How should one test? When should one test? And, when should one stop testing? In other words, how should one select a VVT strategy and how it be optimized? The book is organized in three parts: The first part provides introductory material about systems and VVT concepts. This part presents a comprehensive explanation of the role of VVT in the process of engineered systems (Chapter-1). The second part describes 40 systems' development VVT activities (Chapter-2) and 27 systems' post-development activities (Chapter-3). Corresponding to these activities, this part also describes 17 non-testing systems' VVT methods (Chapter-4) and 33 testing systems' methods (Chapter-5). The third part of the book describes ways to model systems' quality cost, time and risk (Chapter-6), as well as ways to acquire quality data and optimize the VVT strategy in the face of funding, time and other resource limitations as well as different business objectives (Chapter-7). Finally, this part describes the methodology used to validate the quality model along with a case study describing a system's quality improvements (Chapter-8). Fundamentally, this book is written with two categories of audience in mind. The first category is composed of VVT practitioners, including Systems, Test, Production and Maintenance engineers as well as first and second line managers. The second category is composed of students and faculties of Systems, Electrical, Aerospace, Mechanical and Industrial Engineering schools. This book may be fully covered in two to three graduate level semesters; although parts of the book may be covered in one semester. University instructors will most likely use the book to provide engineering students with knowledge about VVT, as well as to give students an introduction to formal modeling and optimization of VVT strategy.

Electronic Design Automation

Synthesis, Verification, and Test

Morgan Kaufmann This book provides broad and comprehensive coverage of the entire EDA flow. EDA/VLSI practitioners and researchers in need of fluency in an "adjacent" field will find this an invaluable reference to the basic EDA concepts, principles, data structures, algorithms, and architectures for the design, verification, and test of VLSI circuits. Anyone who needs to learn the concepts, principles, data structures, algorithms, and architectures of the EDA flow will benefit from this book. Covers complete spectrum of the EDA flow, from ESL design modeling to logic/test synthesis, verification, physical design, and test - helps EDA newcomers to get "up-and-running" quickly Includes comprehensive coverage of EDA concepts, principles, data structures, algorithms, and architectures - helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books, including Test compression, ESL design modeling, large-scale floorplanning, placement, routing, synthesis of clock and power/ground networks - helps readers to design/develop testable chips or products Includes industry best-practices wherever appropriate in most chapters - helps readers avoid costly mistakes

The e Hardware Verification Language

Springer Science & Business Media I am glad to see this new book on the e language and on verification. I am especially glad to see a description of the e Reuse Methodology (eRM). The main goal of verification is, after all, finding more bugs quicker using given resources, and verification reuse (module-to-system, old-system-to-new-system etc.) is a key enabling component. This book offers a fresh approach in teaching the e hardware verification language within the context of coverage driven verification methodology. I hope it will help the reader und- stand the many important and interesting topics surrounding hardware verification. Yoav Hollander Founder and CTO, Verisity Inc. Preface This book provides a detailed coverage of the e hardware verification language (HVL), state of the art verification methodologies, and the use of e HVL as a facilitating verification tool in implementing a state of the art verification environment. It includes comprehensive descriptions of the new concepts introduced by the e language, e language syntax, and its as- ciated semantics. This book also describes the architectural views and requirements of verifi- tion environments (randomly generated environments, coverage driven verification environments, etc.), verification blocks in the architectural views (i. e. generators, initiators, c- lectors, checkers, monitors, coverage definitions, etc.) and their implementations using the e HVL. Moreover, the e Reuse Methodology (eRM), the motivation for defining such a gui- line, and step-by-step instructions for building an eRM compliant e Verification Component (eVC) are also discussed.

Better Software. Faster!

Best Practices in Virtual Prototyping

Happy About The recent rise of "smart" products has been made possible through tight co-design of hardware and software. The growing amount of software and hence processors in applications all around us allows for increased flexibility in the application functionality through its life cycle. Not so long ago a device felt outdated after you owned it for a couple of months. Today, a continuous stream of new software applications and updates make products feel truly "smart". The result is an almost magical user experience where the same product can do more today than it could do yesterday.
In this book we dive deep into a key methodology to enable concurrent hardware/software development by decoupling the dependency of the software development from hardware availability: virtual prototyping. The ability to start software development much earlier in the design cycle drives a true "shift-left" of the entire product development schedule and results in better products that are available earlier in the market.

Throughout the book, case studies illustrate how virtual prototypes are being deployed by major companies around the world. If you are interested in a quick feel for what virtual prototyping has to offer for practical deployment, we recommend picking a few case studies to read, before diving into the details of the methodology.

Of course, this book can only offer a small snapshot of virtual prototype use cases for faster software development. However, as most software bring-up, debug and test principles are similar across markets and applications, it is not hard to realize why virtual prototypes are being leveraged whenever software is an intrinsic part of the product functionality, after reading this book.

Timing Verification of Application-specific Integrated Circuits (ASICs)

Reviewers tell us that Case/Fair is one of the all-time bestselling principles of economics texts because they trust it to be clear, thorough and complete. This well-respected author team is joined for the 9th edition by a new co-author, Sharon Oster. Sharon's research and teaching experience brings new coverage of modern topics and an applied approach to economic theory, as demonstrated in the new Economics in Practice feature. Introduction to Economics; Concepts and Problems in Macroeconomics; The Core of Macroeconomic Theory; Further Macroeconomic Issues; The World Economy For those looking for a trusted and authoritative principles of macroeconomics text that focuses on international econmies as well as the Keynesian Cross. Case/Fair/Oster believe strongly, that a text should use the Keynesian Cross carefully and systematically, to build up to the AD/AS model. One of the great benefits of this approach, is that students of economics won't mistakenly apply what they learned about simple demand and supply to aggregate demand & supply. (A detailed summary of this approach can be found in the preface).

The Designer's Guide to VHDL

Morgan Kaufmann VHDL, the IEEE standard hardware description language for describing digital electronic systems, has recently been revised. The Designer's Guide to VHDL has become a standard in the industry for learning the features of VHDL and using it to verify hardware designs. This third edition is the first comprehensive book on the market to address the new features of VHDL-2008. First comprehensive book on VHDL to incorporate all new features of VHDL-2008, the latest release of the VHDL standard Helps readers get up to speed quickly with new features of the new standard Presents a structured guide to the modeling facilities offered by VHDL Shows how VHDL functions to help design digital systems Includes extensive case studies and source code used to develop testbenches and case study examples Helps readers gain maximum facility with VHDL for design of digital systems

A Comprehensive Physically Based Approach to Modeling in Bioengineering and Life Sciences

Academic Press A Comprehensive Physically Based Approach to Modeling in Bioengineering and Life Sciences provides a systematic methodology to the formulation of problems in biomedical engineering and the life sciences through the adoption of mathematical models based on physical principles, such as the conservation of mass, electric charge, momentum, and energy. It then teaches how to translate the mathematical formulation into a numerical algorithm that is implementable on a computer. The book employs computational models as synthesized tools for the investigation, quantification, verification, and comparison of different conjectures or scenarios of the behavior of a given compartment of the human body under physiological and pathological conditions. Presents theoretical (modeling), biological (experimental), and computational (simulation) perspectives Features examples, exercises, and MATLAB codes for further reader involvement Covers basic and advanced functional and computational techniques throughout the book

Open Verification Methodology Cookbook

Springer Science & Business Media Functional verification is an art as much as a science. It requires not only creativity and cunning, but also a clear methodology to approach the problem. The Open Verification Methodology (OVM) is a leading-edge methodology for verifying designs at multiple levels of abstraction. It brings together ideas from electrical, systems, and software engineering to provide a complete methodology for verifying large scale System-on-Chip (SoC) designs. OVM defines an approach for developing testbench architectures so they are modular, configurable, and reusable. This book is designed to help both novice and experienced verification engineers master the OVM through extensive examples. It describes basic verification principles and explains the essentials of transaction-level modeling (TLM). It leads readers from a simple connection of a producer and a consumer through complete self-checking testbenches. It explains construction techniques for building configurable, reusable testbench components and how to use TLM to communicate between them. Elements such as agents and sequences are explained in detail.

Functional Verification of Dynamically Reconfigurable FPGA-based Systems

Springer This book analyzes the challenges in verifying Dynamically Reconfigurable Systems (DRS) with respect to the user design and the physical implementation of such systems. The authors describe the use of a simulation-only layer to emulate the behavior of target FPGAs and accurately model the characteristic features of reconfiguration. Readers are enabled with this simulation-only layer to maintain verification productivity by abstracting away the physical details of the FPGA fabric. Two implementations of the simulation-only layer are included: Extended Re Channel is a System C library that can be used to check DRS designs at a high level; ReSim is a library to support RTL simulation of a DRS reconfiguring both its logic and state. Through a number of case studies, the authors demonstrate how their approach integrates seamlessly with existing, mainstream DRS design flows and with well-established verification methodologies such as top-down modeling and coverage-driven verification.

SystemVerilog for Verification

A Guide to Learning the Testbench Language Features

Springer Science & Business Media Based on the highly successful second edition, this extended edition of SystemVerilog for Verification: A Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill. In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students' understanding of the material. Other features of this revision include: New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard Descriptions of UVM features such as factories, the test registry, and the configuration database Expanded code samples and explanations Numerous samples that have been tested on the major SystemVerilog simulators SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.

Formal Verification

An Essential Toolkit for Modern VLSI Design

Morgan Kaufmann Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity. Learn formal verification algorithms to gain full coverage without exhaustive simulation Understand formal verification tools and how they differ from simulation tools Create instant test benches to gain insight into how models work and find initial bugs Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems

The Principles of Integrated Technology in Avionics Systems

Academic Press The Principles of Integrated Technology in Avionics Systems describes how integration can improve flight operations, enhance system processing efficiency and equip resource integration. The title provides systematic coverage of avionics system architecture and ground system integration. Looking beyond hardware resource sharing alone, it guides the reader through the benefits and scope of a modern integrated avionics system. Integrated technology enhances the performance of organizations by improving system capacity and boosting efficiency. Avionics systems are the functional center of aircraft systems. System integration technology plays a vital role in the complex world of avionics and an integrated avionics system will fully-address systems, information and processes. Introduces integration technology in complex avionics systems Guides the reader through the scope and benefits of avionic system integration Gives practical guidance on using integration to optimize an avionics system Describes the basis of avionics system architecture and ground system integration Presents modern avionics as a system that is becoming increasingly integrated

Functional Verification of an ALU Core Applying the Constrained Random Approach

ASIC complexity is increasing so rapidly that designer productivity is not coping with the growth. Verification presents about 60-70% of the total design effort and only advances in verification methodology can improve the time to market considerably. Directed tests and 'golden' reference files will soon become the primitive tools of the modern test environment. Verification engineers are consequently looking towards new methodologies like Constrained-Random approach to reduce test bench development time, and speed-up the time it takes to achieve complete verification of their ASIC or SoC. Test bench automation tools for constrained-random stimulus generation and functional coverage create tests for corner cases that even engineers who designed the system may not anticipate and hence find bugs early in the development cycle. This thesis describes the study and implementation of the Constrained-Random concept in the Functional verification of a 32-bit ALU core using Specman.

Deductive Software Verification – The KeY Book

From Theory to Practice

Springer Static analysis of software with deductive methods is a highly dynamic field of research on the verge of becoming a mainstream technology in software engineering. It consists of a large portfolio of - mostly fully automated - analyses: formal verification, test generation, security analysis, visualization, and debugging. All of them are realized in the state-of-art deductive verification framework KeY. This book is the definitive guide to KeY that lets you explore the full potential of deductive software verification in practice. It contains the complete theory behind KeY for active researchers who want to understand it in depth or use it in their own work. But the book also features fully self-contained chapters on the Java Modeling Language and on Using KeY that require nothing else than familiarity with Java. All other chapters are accessible for graduate students (M.Sc. level and beyond). The KeY framework is free and open software, downloadable from the book companion website which contains also all code examples mentioned in this book.

The Elements of Journalism

What Newspeople Should Know and the Public Should Expect

Crown In July 1997, twenty-five of America's most influential journalists sat down to try and discover what had happened to their profession in the years between Watergate and Whitewater. What they knew was that the public no longer trusted the press as it once had. They were keenly aware of the pressures that advertisers and new technologies were putting on newsrooms around the country. But, more than anything, they were aware that readers, listeners, and viewers — the people who use the news — were turning away from it in droves. There were many reasons for the public's growing lack of trust. On television, there were the ads that looked like news shows and programs that presented gossip and press releases as if they were news. There were the "docudramas," television movies that were an uneasy blend of fact and fiction and which purported to show viewers how events had "really" happened. At newspapers and magazines, celebrity was replacing news, newsroom budgets were being slashed, and editors were pushing journalists for more "edge" and "attitude" in place of reporting. And, on the radio, powerful talk personalities led their listeners from sensation to sensation, from fact to fantasy, while deriding traditional journalism. Fact was blending with fiction, news with entertainment, journalism with rumor. Calling themselves the Committee of Concerned Journalists, the twenty-five determined to find how the news had found itself in this state. Drawn from the committee's years of intensive research, dozens of surveys of readers, listeners, viewers, editors, and journalists, and more than one hundred intensive interviews with journalists and editors, The Elements of Journalism is the first book ever to spell out — both for those who create and those who consume the news — the principles and responsibilities of journalism. Written by Bill Kovach and Tom Rosenstiel, two of the nation's preeminent press critics, this is one of the most provocative books about the role of information in society in more than a generation and one of the most important ever written about news. By offering in turn each of the principles that should govern reporting, Kovach and Rosenstiel show how some of the most common conceptions about the press, such as neutrality, fairness, and balance, are actually modern misconceptions. They also spell out how the news should be gathered, written, and reported even as they demonstrate why the First Amendment is on the brink of becoming a commercial right rather than something any American citizen can enjoy. The Elements of Journalism is already igniting a national dialogue on issues vital to us all. This book will be the starting point for discussions by journalists and members of the public about the nature of journalism and the access that we all enjoy to information for years to come.

Validation, Verification, and Testing of Computer Software

Analog-Mixed Signal Verification

Createspace Independent Publishing Platform Introduction The purpose of this book is to provide insight and intuition into the analog and analog-mixed signal system verification. It is also a journey the author of this book has been through on the way to tackle practical design and verification challenges with state of art analog and mixed signal designs. Motivation for authoring this book The digital design verification skill set is very different than analog design and verification. Traditionally, the analog block level verification is performed by the analog designers, and digital design verification is performed by digital design verification engineer. Lack of cross domain skill set makes it challenging to perform verification at mixed-signal level. Hence, either analog designer engineer should learn advanced digital verification techniques or digital design verification engineer embrace analog

verification to become analog-mixed signal verification engineer. This book is written keeping this new trend in mind, hence it covers digital design fundamentals, digital design verification as well as analog design fundamentals, and analog performance verification. Organization of this book Keeping the readers of analog verification or digital design verification background in mind, the book has first 5 chapters focused on the fundamentals of the analog design, digital design, and its verification. Chapter 6 and chapter 7 focuses on the analog-mixed signal design verification and behavioral modeling respectively. Chapter 8 is dedicated to the low power verification techniques. Chapter 1: Introduction to Analog Mixed Signal Verification This chapter discusses about the evolution of the verification methodologies, history of analog-mixed signal designs, applications, and future trends. Chapter 2: Analog Design Fundamentals The purpose of this chapter is to give an overview of the analog design fundamentals for digital design background engineers. Major focus is given on analog behavior, design criteria and their concept rather than design themselves, such as voltage/current reference, some of the basic key analog design properties such as gain, band width, basics of jitter, eye diagram, etc. Chapter 3: Digital Design Fundamentals In this chapter, we explain digital design flow, combinational and sequential logic design fundamentals, design for testability, concepts of timing, and timing verification. Chapter 4: Analog Verification This chapter focuses on analog performance verification and functional verification under the context of mixed signal design hierarchical verification rather than the detail performance analysis of the designs themselves. Chapter 5: Digital Design Verification This chapter explains the tools and methodologies that are evolved over the period that are predicated on predictable quality and verification efficiency. The chapter contains the sections on the coverage driven verification (CDV) methodology, assertion based verification (ABV) methodology, and overview of the CDV using Open Verification Methodology (OVM). Chapter 6: Analog-Mixed Signal Verification This chapter discusses about the AMS verification phases, choosing the right abstraction of DUT for a given verification challenge, AMS verification planning, testplanning for AMS design verification, and testbench development with re-use in mind. Chapter 7: Analog Behavioral Modeling This chapter explains about the applications of analog behavioral models, modeling methodology, simple examples of various analog behavioral modeling styles, selection of accuracy level of the models based on the verification plan, model verification, and signoff. Chapter 8: Low Power Verification The purpose of this chapter is to explain the low power design verification challenges, key low power design elements, low power design techniques, low power design and verification cycle, testplanning for low power design verification, power aware digital, and AMS simulations.

Software Abstractions

Logic, Language, and Analysis

MIT Press In Software Abstractions Daniel Jackson introduces an approach to software design that draws on traditional formal methods but exploits automated tools to find flaws as early as possible. This approach -- which Jackson calls "lightweight formal methods" or "agile modeling" -- takes from formal specification the idea of a precise and expressive notation based on a tiny core of simple and robust concepts but replaces conventional analysis based on theorem proving with a fully automated analysis that gives designers immediate feedback. Jackson has developed Alloy, a language that captures the essence of software abstractions simply and succinctly, using a minimal toolkit of mathematical notions. This revised edition updates the text, examples, and appendixes to be fully compatible with Alloy 4.